Tyndall
National Institute
Institiúid Náisiúnta

# E-Beam Lithography

State-of-the-art facilities. Dedicated people

The e-beam lithography laboratory provides small geometry lithography facilities to all of the other areas. It is the only area that has 2 way wafer exchange between all of the other laboratories. The system has substrate/wafer holders dedicated to samples from the other main processing facilities, silicon and compound semiconductors, this ensures no cross contamination between the laboratories. The e-beam system can handle substrate sizes from small pieces to full 200mm wafers.

## Lithography System

The e-beam system is a Jeol 6000FS lithography tool.

Writing Characteristics:

- Beam shape: Spot Beam
- Emitter: ZrO/W TFE Source
- Acceleration Voltage: 25kV/50kV
- Stage Movement: Vector Scan

Above: Jeol 6000FS Electron beam lithography system

## Laboratory Facilities

The e-beam lithography area is equipped with its own resist spin, bake and develop equipment. Because of the low throughput requirements for the e-beam the spin and develop equipment is SSE OPTIcoat manual systems. Alternative equipment is also available in all of the other three processing laboratories. The system chamber is located in a class 100 cleanroom.

## Additional Software

For dense patterns the system is also equipped with CAPROX® proximity correction software from SIGMA-C, should it be needed.

## Integration

An e-beam system is not of much use as a standalone processing tool. It must be integrated with the process facilities of the other laboratories. In silicon processing a system of “mix-and-match” processing has been developed in combination with the Ultratech Stepper. This means that critical layers such as gate definition can be carried out on the e-beam system and the larger geometry less critical lithography can be done on the stepper.

Resist and etch processes have been developed combining the e-beam lithography and the etch tools in the Microsystems laboratory, STS ASE DRIE and in the silicon laboratory with the Aviza M0RI dielectric/polysilicon etch system.

There is also an e-beam resist, lift-off process for metals that are evaporated in the compound semiconductor laboratory. This process can be used with either compound semiconductor substrates or silicon, but silicon substrates cannot be returned to the silicon laboratory following metal deposition.

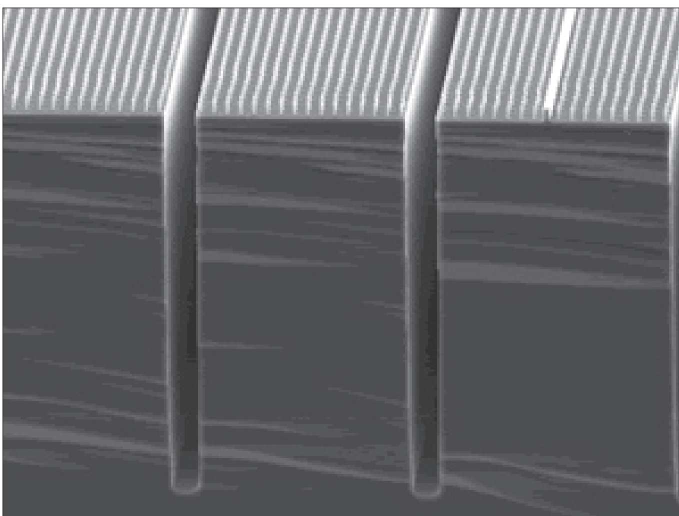
## Specifications

| | |
|---|---|
| Beam Current Density: | Max. 2000A/cm$^2$ (50kV)<br>Max. 1000 A/cm$^2$ (25kV) |
| Min. Spot Size: | 5nm |
| Scanning Speed: | 12MHz |
| Field Size: | 1600µm (25kV/4th Lens)<br>800µm (50kV/4th Lens)<br>160µm (25kV/5th Lens)<br>80µm (50kV 5th Lens) |
| Increment: | 25nm (25kV/4th Lens)<br>12.5nm (50kV/4th Lens)<br>2.5nm (25kV/5th Lens)<br>1.25nm (50kV 5th Lens) |

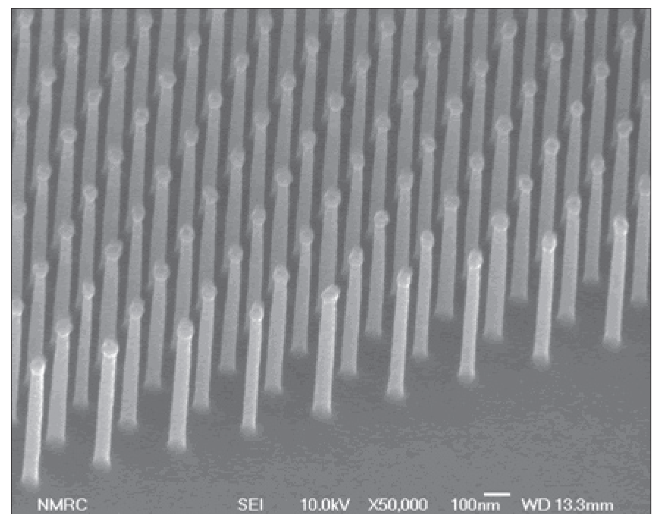
## Direct Write Performance

| | |
|---|---|
| Field Stitching Accuracy: | 0.06µm(2σ)) (25kV/4th Lens)<br>0.04µm(2σ) (50kV/5th Lens) |
| Overlay Accuracy: | 0.06µm(2σ) (25kV/4th Lens)<br>0.04µm(2σ) (50kV/5th Lens) |
| Minimum Linewidth: | 20nm<br>10nm attainable |

Above: Loading the substrate holder magazine on the Jeol 6000FS



Above: 170µm deep channels with 1µm diameter, 5µm tall pillars patterned using the e-beam and etched on the STS ASE DRIE tool.




Above: Silicon pillars 60nm in diameter and 600nm tall, e-beam resist still on top of the pillars

**For More Information on these topics contact:**

Brendan McCarthy
E: brendan.mccarthy@tyndall.ie
T: +353 21 4904423