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## **NAP Annual Scientific Workshop 25<sup>th</sup> January 2007**

### **Presenter**

**Chris Murray – CRANN, TCD**

### **Project Title**

**Production of thin Si membranes using  
SOI wafers**





**NAP 49/50**

Chris Murray

January 25<sup>th</sup> 2007

## Outline

Motivation for the project

Required deliverables

Timeline

Results to date

Summary



## Motivation – Moore’s Law into the Future

### Evolutionary CMOS

- continued scaling of CMOS to 32nm node- 2009
- Lithography, high k dielectrics, metal gates etc

### Revolutionary CMOS

- 32-16nm node 2011-2019
- monolithic integration of new technologies with CMOS – ‘enhanced’ CMOS. Taking it to the limit!
- 3D architectures such as FINFET
- 1D materials – Nanowires and carbon nanotubes

### Beyond CMOS

- 16nm node – 6nm gate length around 2020!
- Logical state other than electron charge
- New materials, devices, nano-architectures and system innovations
- Many options available - Molecular electronics, **Spintronics** etc



## What is required?

### Requirements

- Integration on or with CMOS
- Scalable for several generations beyond CMOS
- High information/signal processing throughput
- Energy dissipation per operation ‘substantially’ less than CMOS
- Room temperature operation
- Gain!

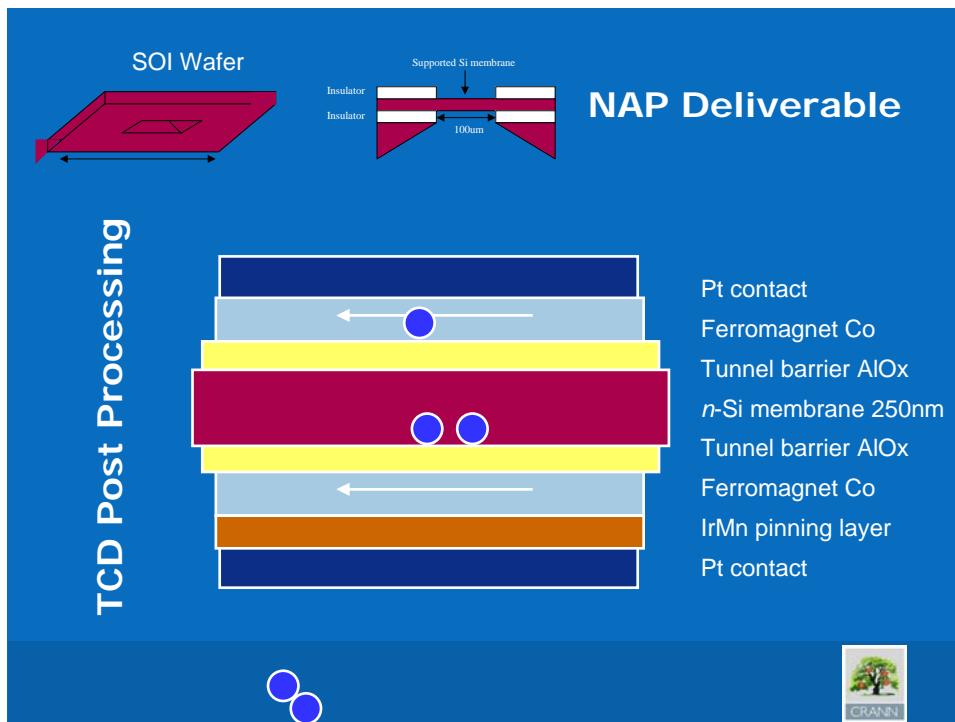
### Story so far:

- People have demonstrated combinations of optical and electrical injection/detection of spin polarised currents in SC channel (usually III-V)
- No-one has demonstrated purely electrical injection and detection in Si channel

### Goal

- Demonstrate electrical spin injection and detection in a silicon channel at room temperature using tunnel barriers and metallic ferromagnets





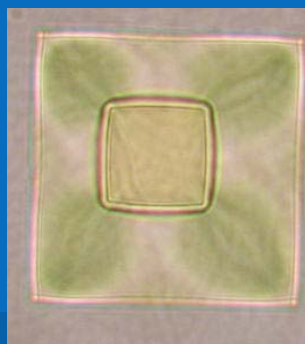
## Project Deliverables

### NAP49

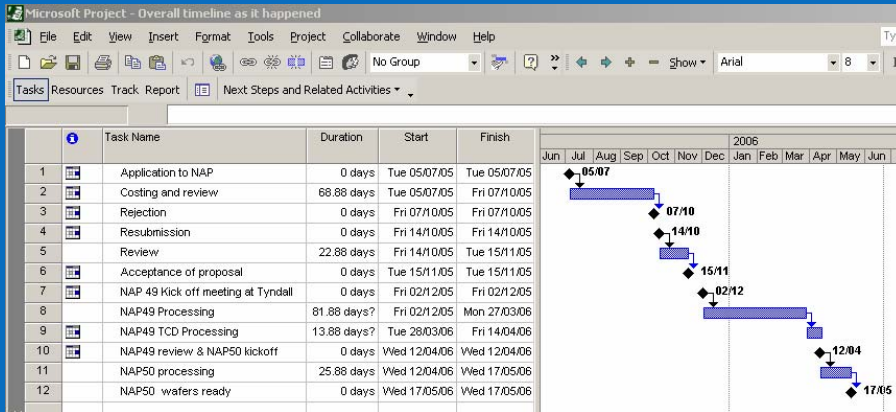
- Process validation run
- 250nm thick Si membranes from standard p-SOI
- No implant – non-functional
- 5-100um side
- Mask creation
- Double sided processing
- Bulk Si micromachining
- Deliver 5 wafers, 200 membranes/wafer
- TCD to post process and review
- Go/No go for NAP50

### NAP50

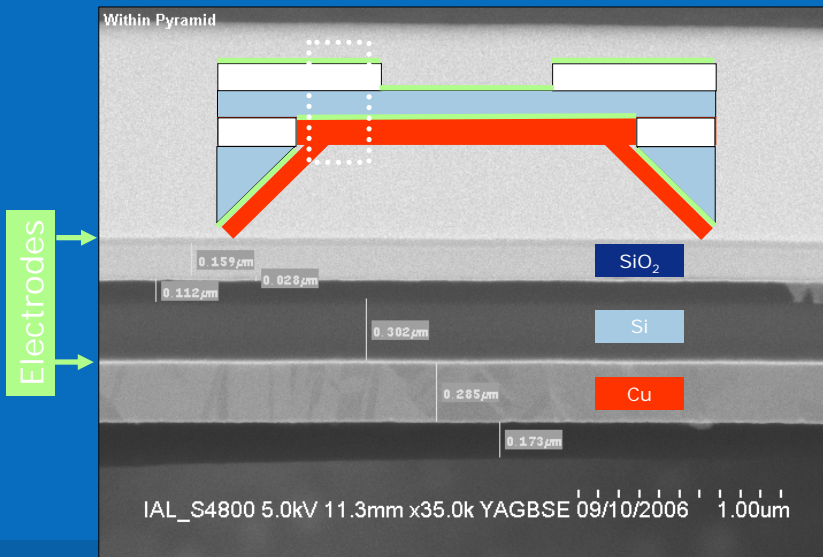
- Eliminate any bugs in NAP49
- Deliver implanted n-Si membranes using same mask set
- $1e11-1e16$  cm<sup>-2</sup> phosphorous dose
- Deliver 10 wafers, 205 devices each



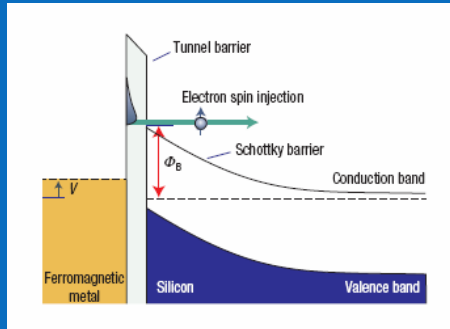
# Timeline



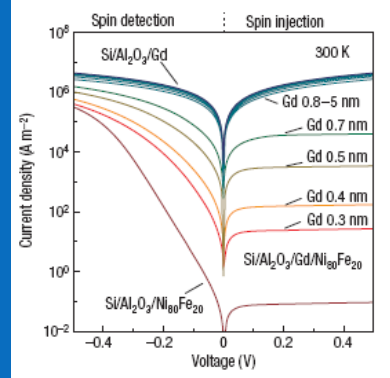
# IAL Hi-Res SEM Images



## Next Steps-Reducing the Schottky barrier



$$\phi_B = \Phi_M - \chi$$



Min et al, Nature Materials, 5, 817-822, (2006)

Curie temp of Gd=296K



## Summary

- NAP49/50 involved the processing of thin doped n-Si membranes from SOI for spintronics experiments in TCD/CRANN
- Unable to source similar processing elsewhere
- Initial application was rejected after approx. 10 weeks
- Follow-up application was successful
- Some frontside damage to NAP49 wafers, fixed in NAP50
- Delivery of NAP50 wafers very prompt
- All post processing and measurement carried out at CRANN/Intel
- Initial results did not achieve goal, but inclusion of Gd interlayers shown to reduce Schottky barrier
- NAP project enables this research
- Future collaboration likely

## Acknowledgements

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